Greg Tumbush, Ph.D., P.E.
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Summary: 20 years of experience in all aspects of ASIC and FPGA design and verification from concept to silicon validation

QUALIFICATIONS

- Designs: ARM interfaces, FPGA protyping, low-power digital processor, low-power wireless interface core, low-power CODEC. SystemC models of processor, memory management unit, etc. Led international design teams.
- Verification: From scratch UVM-based coverage driven verification environments, mixed signal verification environments both at the block level and full-chip level. Developed Real-Number models of analog blocks. Led international verification teams.
- Languages: Fluent in UVM, SystemVerilog**,** VHDL, SystemC, C/C++, Perl, Python, UNIX, and shell scripts.
- CAD Tools: Well versed in Synopsys's Spyglass CDC, Design Compiler, Primetime, TetraMax, Power Compiler, Z01X, CustomSim XA, and Formality tools as well as Cadence's Conformal, Incisive, and AMS tools. Also familiar with Mentor's QuestaSim and Xilinx ISE and Vivado tools.
- Bus Protocols: Highly knowledgeable of SPI, ARM High Speed Bus (AHB), and I^2C protocols.

EMPLOYMENT HISTORY

July/18-Present EM Microelectronics US, Digital Design/Verification Engineer
EM Micro specializes in ultra low power ASICs for the consumer market.

- Verification of 4^{th} generation image processing ASIC.
- Led international multi-site effort to evaluate Cadence JasperGold Formal tool
- Silicon validation of toll road transponder ASIC
- Utilized Synopsys Spyglass Clock Domain Crossing (CDC) tool to determine CDC weaknesses in toll road transponder ASIC
- Implemented design changes, timing closed, and formally proved with Synopsys Formality metal changes for 2^{nd} spin of toll road transponder ASIC

Aug/08-July/18 Tumbush Enterprises LLC, Owner
Consulting company specializing in advanced design and verification in the low power ASIC industry.

- Major contributor on 14 successful mixed signal ASIC tapeouts.

- Verified, at the chip level, the 1st generation of a toll road transponder ASIC for current consumption and RF transmit and receive operation using Synopsys CustomSim XA simulator. Led multi-site verification team.
- Designed major blocks of a 3rd generation sensor hub ASIC. Developed and maintained FPGA prototype of ASIC. Led multi-site international verification team.
- Verified, at the chip level, the 2nd and 3rd generations of an image processing ASIC using Cadence AMS. Developed and verified Real-Number models of analog blocks using Cadence AMS. Led multi-site verification team.
- Designer of 2nd generation sensor hub ASIC. Updated device and design spec. Synthesized, performed STA, equivalency checking. Closed timing with layout.
- Verified mixed signal RFID ASIC using AMS.
- Architect of mixed signal ASIC, verifying system using UVM and SystemVerilog.
- Digital design lead on sensor hub ASIC using Synopsys ARC core. Performed STA using PrimeTime, synthesis using DesignCompiler, test pattern generation using TetraMax.
- Verified custom CPU for 1st generation image processing ASIC using UVM and SystemVerilog, verification lead for ASIC.
- Verification using an object oriented SystemVerilog testbench for an antenna capacitor matching ASIC for the cell phone market.
- Verilog design and verification with SystemVerilog for a 2nd glucose monitor ASIC with an embedded ARM core. Wrote firmware to test ASIC.
- Verilog design, verification with SystemVerilog, STA using PrimeTime, synthesis using DesignCompiler, and equivalency checking using LEC for a glucose monitor ASIC with an embedded ARM core. Wrote firmware to test ASIC.
- Developed SystemVerilog testbenches and wrote tests for hearing aid ASIC.
- Performed 100% of Verilog design, verification with SystemVerilog, STA using PrimeTime, synthesis using DesignCompiler, equivalency checking using LEC, and scan pattern generation using TetraMax for a patient monitoring ASIC.

Aug/08-May/14 University of Colorado, Colorado Springs, ½ time instructor, Adjunct
Develop and instruct senior/graduate level courses in digital design methodology, verification using SystemVerilog and UVM, and rapid prototyping using FPGA's.

Mar/03-Aug/08 Starkey Labs, AMI Semi, ON Semi, Senior Digital Design Engineer
ON Semiconductor purchased AMI Semiconductor in '07
AMI Semiconductor purchased the Starkey Labs Design Center in July '06.

- Digital lead on numerous mixed signal medical ASIC's.
- Managed international teams of designers.
- Expanded use of SystemVerilog methodology to include functional coverage and assertions using SVA.
- Architected, designed and delivered on-schedule a very complex wireless interface module.

- Implemented a CODEC which included Wave Digital Filters, Sigma-Delta, and Pulse-Width Modulators, and slink filters.
- Explored architectures for CODEC using Synopsys Design Compiler and Power Compiler for minimum area/power.
- Architected and designed numerous blocks in SystemC.
- Developed a co-verification methodology for a DSP modeled in SystemC.
- Nominated for Performance Award in 2004

Feb/00-July/02 Astek Corporation, Lead ASIC Design Engineer
Astek Corporation is a small company specializing in the design of ASICs and FPGAs both in-house and on contract.

- Worked on nine major commercial projects.
- Designed and verified blocks using PCI, SCSI, AHB, and FiberChannel protocols.
- Synthesized ASICs with Synopsys Design Compiler, analyzed timing with Synopsys Primetime, and equivalency checking with Verplex Conformal lec.
- Mentored junior engineers and managed small design teams.
- Recruited and interviewed nine new employees.

March/93-Sept/94 March/98-June/99 USAF Research Lab, Computer Engineer

- Led technical effort to prove validity of accelerating DSP and graphics algorithms on FPGA based reconfigurable computing platform.
- Designed DSP cores in VHDL, simulated using ModelSim, and synthesized with Synplify.
- Managed $5 million in Air Force Research Laboratory programs with Synopsys, Inc., Lucent Technologies, and various subcontractors.

EDUCATION

- **Ph.D. Computer Engineering**, March/98, University of Cincinnati, Dissertation Title – "Partitioning under Multiple Constraints", Focus: Design Automation
- **M.S. Electrical Engineering**, March/93, The Ohio State University, Thesis Title – "Verification and Integration of a CMOS Process for CAD", Focus: VLSI Design and Computer Aided Design
- **B.S. Electrical Engineering**, June/91, Graduated Cum Laude, Wright State University, Focus: Digital Design

Publications

See http://tumbush.com/published_papers/published_papers.html for publications.

Professional Organizations

1. Technical program committee Design and Verification Conference (DVCON), 2005-2007, 2009-present
2. Co-Chair North American SystemC Users Group (NASCUG), Summer 2005/2006 and Spring 2006.