# A 2mW 400MHz RF Transceiver SoC in 0.18um CMOS Technology for Wireless Medical Applications

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***Abstract* — An ultra low power 400MHz 128kbps-FSK RF transceiver SoC which consumes less than 2mA from a 1V supply was implemented in a 0.18µm CMOS technology for wireless medical applications and applied to a wireless hearing aid communication system, a new generation of hearing aid device. The transceiver was implemented fully differentially and directly matched to a non-50ohm miniaturized dipole antenna. The receiver sensitivity of -93dBm (BER=$10^{-3}$) was measured for 128Kbps data rate. The transceiver architecture has the ability of selection of image band in receive mode and transmitting in the image band in transmit mode. The whole RF transceiver including digital modulator and demodulator occupies a die area of less than 2.6mm$^2$.**

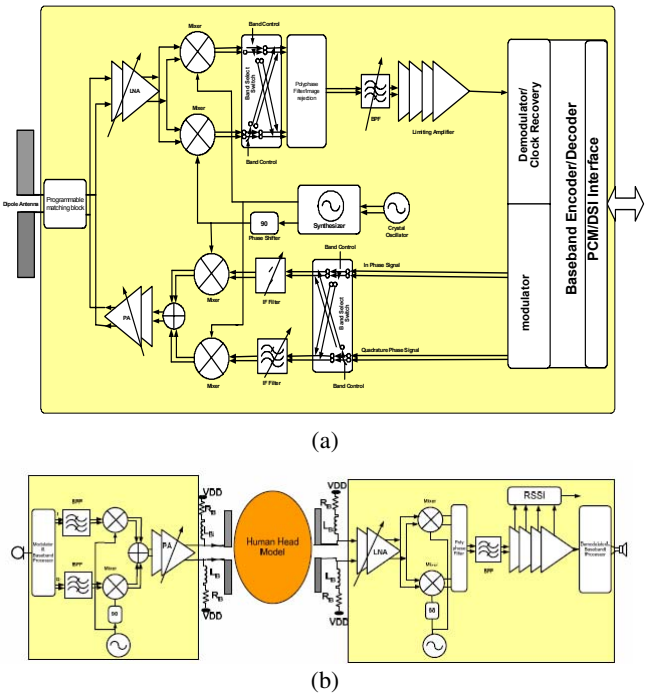
***Index Terms* — CMOS, transceiver, ultra low power, direct matching.**

## I. Introduction

The need for ultra low power and compact radios for medical and related products is growing rapidly. The requirements in this market for low voltage (battery operated), ultra low current (long life), miniaturized antenna and RF performance push the bounds of current technologies and existing solutions that maybe applicable to medical applications [1,2]. The design of such products requires a holistic approach. It is critical to consider all aspects of the design from antenna and system architecture to circuit level design up-front. For instance, electing to use a 50 Ohm antenna system may be beneficial for "off-the-shelf" component selection, but constrain the design of the power amplifier (PA) and low noise amplifier (LNA) sections to have more complex matching circuits and consume higher power. The applications in the medical field, also typically constrain in terms of off-chip component counts and antenna dimension and so high levels of integration are necessary in any selected architectures. The system/architecture trade-offs, as discussed in this paper, are then critical to a successful product for wireless medical applications.

This paper presents an ultra low power transceiver SoC in a 0.18µm CMOS technology and operating with a 1V supply, for wireless medical and related applications such as hearing aid to hearing aid and a remote device to hearing aid communication. Section II is a discussion of the low power transceiver architecture. Section III describes the main circuit blocks of the transceiver. Section IV presents measurement and test results while conclusions are given in section V.

## II. Transceiver Architecture



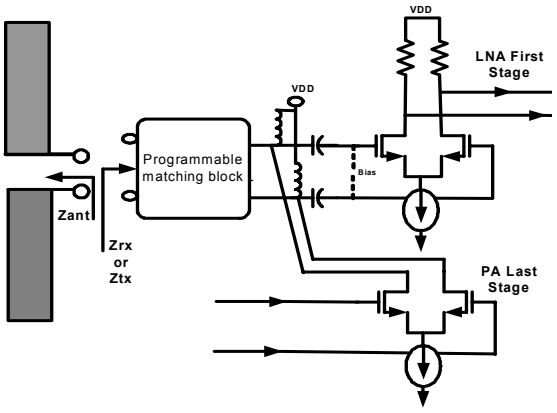

(a)

(b)

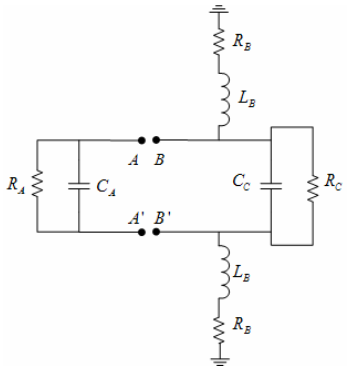
Fig. 1. a) Transceiver block diagram b)A simplified block diagram of the designed wireless hearing aid system for ear to ear communication using transceiver in (a).

Fig.1 shows the block diagram of the SoC. Direct matching of a miniaturized dipole antenna to the transceiver chip, fully differential implementation of the front-end including circuit and antenna, ability of selection of image band in receive mode, and transmitting in the image band in transmit mode are the unique features of the transceiver

architecture [3]. A low-IF architecture is used to minimize the power consumption of IF blocks, as well as to avoid the local oscillator self-mixing and flicker noise limitations of zero-IF architecture. By swapping in-phase and quadrature phase before up-conversion, the transmitter can operate in a certain frequency in the band of interest or image of that frequency. In the receive mode, a certain frequency or its image can be selected by swapping in-phase and quadrature phase after down-conversion and before the poly-phase filter. This feature was implemented because the system has to operate inside 402-405MHz band and outside this band by adding minimum complexity into the system.




(a)




(b)

Fig. 2. (a)A schematic of RF front-end of the transceiver (b) The equivalent admittance for the LNA, the bias circuit, and the antenna .

Fig. 2 illustrates the direct matching of the miniaturized dipole antenna to the LNA and PA [4,5]. A programmable matching block is used between the antenna and the transceiver to compensate for variations in antenna impedance when the antenna environment and surrounding objects change. The simplest form of this block is a parallel variable capacitor to tune the resonance frequency of parallel resonance circuit between antenna and transceiver.

## III. Description of the Main Circuit Blocks

In the receive part of the chip, the LNA is directly connected and matched to a miniaturized antenna in the frequency band of interest [4]. The LNA is a differential-input/differential-output amplifier with resistive loads, and is followed by a Gilbert mixer that down-converts the RF signal to the IF frequency of $f_{IF}$=1MHz. The LNA-Mixer pair consumes a total current of about 500 µA, and provides a gain and noise figure of 25 and less than 3 dB, respectively. The mixer is followed by IF amplifier stages that limits the selected signal by a gm-C bandpass filter and provides a digital signal to the input of the demodulator section.

The LO signal is provided by a PLL-based frequency synthesizer with on-chip loop filter that generates a sinusoidal signal at f=810 MHz, which is then divided by two before entering the LO port of the mixer to generate in-phase and quadrature phase LO signals. As depicted in Fig. 3, a cross-coupled LC oscillator with NMOS and PMOS coupled pairs is used to minimize the power consumption of the VCO block. The synthesizer consumes a total current of 800µA and its measured phase noise is demonstrated in Fig. 4.

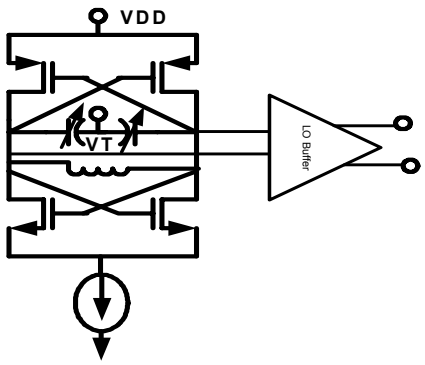



Fig. 3. Circuit diagram of the VCO.

In the transmit part, 1MHz in-phase and quadrature modulated data from the modulator output enter two IF filters. After filtering the signal is upconverted to 400MHz by two I and Q Gilbert mixers and then amplified by the power amplifier and delivered to a high impedance miniaturized antenna with the impedance of about 8Kohm.

The chip has a digital baseband processing block that implements the following functions: framing, error detection and correction coding, interleaving/de-

interleaving, FSK modulation and demodulation, clock recovery, and proprietary encoding and decoding. Further, the chip implements $I^2C$ and PCM interfaces, Enable/Disable and Tx/Rx Select lines.

In order to improve immunity to noise while keeping complexity low, a modified version of Hamming code was chosen for error detection and correction. Along with the interleaving function, the BER performance was improved by about 2dB which was deemed satisfactory for this wireless medical application. To maximize the data throughput, a new proprietary coding scheme was devised and implemented that allows received frames to be recovered with minimal overhead. The overhead associated with this scheme is a maximum of 2 bits out of 128 bits (< 1.6% overhead).

The digital FSK modulator allows the spectrum to be shaped to reduce spectral re-growth, by introducing intermediate frequency steps of variable steps size.

## IV. Measurement Results

Table 1 shows a summary of measured performance of the system. The SoC consumes about 1.7mA in the transmit mode and 2mA in the receive mode from a 1V supply. Sensitivity of -93dBm (BER=$10^{-3}$) was measured for the FSK data rate of 128Kbps. The measured BER versus receive signal level is demonstrated in Fig.5. The die micrograph of the SoC that occupies an area of < 2.6 $mm^2$ is shown in Fig. 6.

Table 1: Summary of measurement results

| **Parameter** | **Value** |
|---|---|
| Supply Voltage | **1.05 V to 1.5V** |
| Maximum Current Consumption | **2mA RX Mode**<br>**1.7mA TX Mode** |
| Temperature Range | **-10° - 55°C** |
| RF Frequency | **404 or 406 MHz** |
| Maximum RF Transmit Power<br>Typical RF Transmit Power | **-12 dBm**<br>**-18 dBm** |
| RX Sensitivity<br>128Kps FSK (BER=$10^{-3}$) | **-93dBm** |
| Die Size | **<2.6mm$^2$** |
| Interfaces | **PCM, DSI, $I^2C$ and Control Lines** |

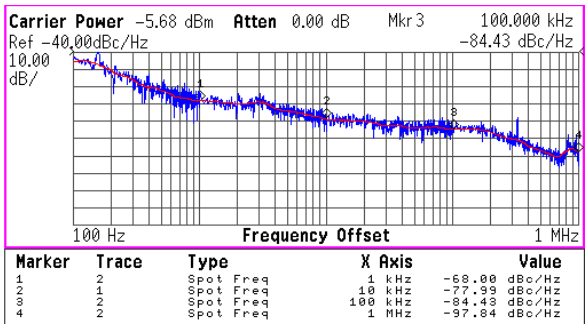



Fig. 4. Measured 810MHz VCO phase noise

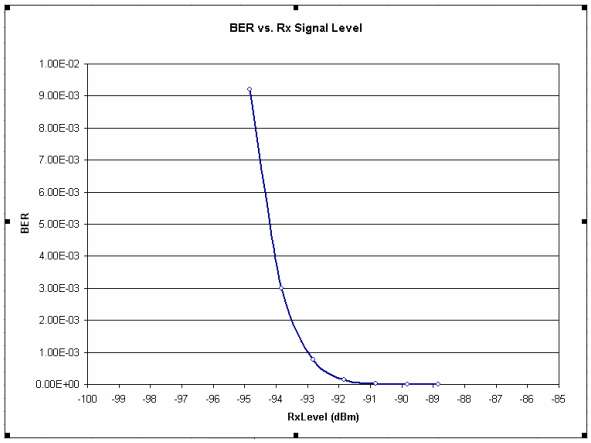



Fig. 5. Measured BER of the full system versus RF signal level at the input of receiver

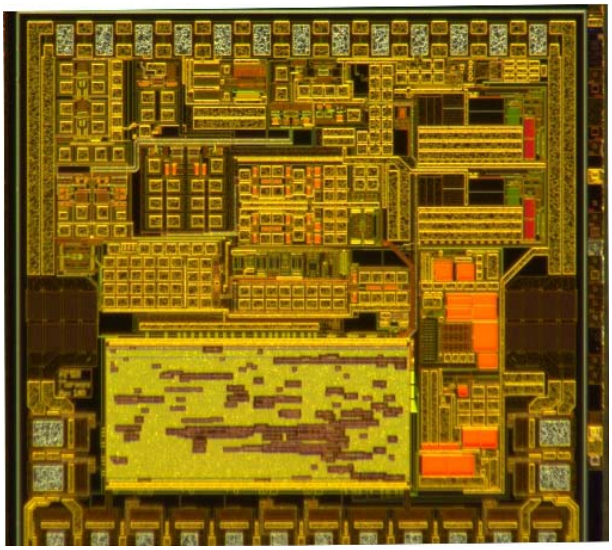


Fig. 6. A die micrograph of the transceiver

## V. Conclusion

An ultra low power transceiver for wireless medical applications was implemented and applied to a wireless hearing aid device for ear to ear communications. The transceiver was directly matched to a non-50ohm miniaturized antenna and to minimize the required matching components between antenna and LNA/PA. Sensitivity of -93dBm was measured for the receiver for the data rate of 128Kbps.

## References


[1] Philip Quinlan et al., "A multimode 0.3-200kb/s transceiver for the 433/868/915MHz bands in 0.25-µm CMOS," IEEE J. Solid-States Circuits, vol. 39, p. 2297-2310, Dec. 2004.

[2] Vincent Peiris et al., "A 1V 433/868MHz 25kb/s-FSK 2kb/s-OOK RF transceiver SoC in standard digital 0.18µm CMOS," ISSCC Dig. Tech. Papers, pp. 258-259, Feb. 2005.

[3] M-R.N-Ahmadi et al., "Low-IF Transceiver Architecture and Antenna," US. P. App. No. 60/972,341. F.:14.09.2007 (patent pending)

[4]G. Shaker et al., "Miniature Antenna for Wireless Communications," US. Patent App. No. 60/992,856. F.:06.12.2007 (patent pending)

[5] G. S. A. Shaker , M.R. Nezhad-Ahmadi, S. Safavi-Naeini1, G. Weale, "Direct matching of a miniaturized antenna to an on-chip low noise amplifier," Accepted to be presented and published in IEEE RWS2008.